UNITED STATES PATENT AND TRADEMARK OFFICE

UNITED STATES DEPARTMENT OF COMMERCE
United States Patent and Trademark Office
Address: COMMISSIONER FOR PATENTS
P.O. Box 1450
Alexandria, Virginia 22313-1450
www.uspto.gov

APPLICATION NO.	FILING DATE	FIRST NAMED INVENTOR	ATTORNEY DOCKET NO.	CONFIRMATION NO.
10/612,129	07/02/2003	Chee Kiang Yew	TI-26239.1	3928

23494 7590 08/06/2004

TEXAS INSTRUMENTS INCORPORATED
P O BOX 655474, M/S 3999
DALLAS, TX 75265

EXAMINER	
CAO, PHAT X	
ART UNIT	PAPER NUMBER
2814	

DATE MAILED: 08/06/2004

Please find below and/or attached an Office communication concerning this application or proceeding.

Office Action Summary	Application No.	Applicant(s)	
	10/612,129	YEW ET AL.	
	Examiner	Art Unit	
	Phat X. Cao	2814	

-- The MAILING DATE of this communication appears on the cover sheet with the correspondence address --

Period for Reply

A SHORTENED STATUTORY PERIOD FOR REPLY IS SET TO EXPIRE 3 MONTH(S) FROM THE MAILING DATE OF THIS COMMUNICATION.

- Extensions of time may be available under the provisions of 37 CFR 1.136(a). In no event, however, may a reply be timely filed after SIX (6) MONTHS from the mailing date of this communication.
- If the period for reply specified above is less than thirty (30) days, a reply within the statutory minimum of thirty (30) days will be considered timely.
- If NO period for reply is specified above, the maximum statutory period will apply and will expire SIX (6) MONTHS from the mailing date of this communication.
- Failure to reply within the set or extended period for reply will, by statute, cause the application to become ABANDONED (35 U.S.C. § 133). Any reply received by the Office later than three months after the mailing date of this communication, even if timely filed, may reduce any earned patent term adjustment. See 37 CFR 1.704(b).

Status

1)☒ Responsive to communication(s) filed on *21 May 2004*.

2a)☒ This action is **FINAL**. 2b)☐ This action is non-final.

3)☐ Since this application is in condition for allowance except for formal matters, prosecution as to the merits is closed in accordance with the practice under *Ex parte Quayle*, 1935 C.D. 11, 453 O.G. 213.

Disposition of Claims

4)☒ Claim(s) *1-15* is/are pending in the application.

4a) Of the above claim(s) _____ is/are withdrawn from consideration.

5)☒ Claim(s) *3* is/are allowed.

6)☒ Claim(s) *1-2, 4-15* is/are rejected.

7)☐ Claim(s) _____ is/are objected to.

8)☐ Claim(s) _____ are subject to restriction and/or election requirement.

Application Papers

9)☐ The specification is objected to by the Examiner.

10)☐ The drawing(s) filed on _____ is/are: a)☐ accepted or b)☐ objected to by the Examiner.

Applicant may not request that any objection to the drawing(s) be held in abeyance. See 37 CFR 1.85(a).

Replacement drawing sheet(s) including the correction is required if the drawing(s) is objected to. See 37 CFR 1.121(d).

11)☐ The oath or declaration is objected to by the Examiner. Note the attached Office Action or form PTO-152.

Priority under 35 U.S.C. § 119

12)☐ Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).

a)☐ All b)☐ Some * c)☐ None of:

1.☐ Certified copies of the priority documents have been received.

2.☐ Certified copies of the priority documents have been received in Application No. _____.

3.☐ Copies of the certified copies of the priority documents have been received in this National Stage application from the International Bureau (PCT Rule 17.2(a)).

* See the attached detailed Office action for a list of the certified copies not received.

Attachment(s)

1) ☐ Notice of References Cited (PTO-892)
2) ☐ Notice of Draftsperson's Patent Drawing Review (PTO-948)
3) ☐ Information Disclosure Statement(s) (PTO-1449 or PTO/SB/08) Paper No(s)/Mail Date _____.
4) ☐ Interview Summary (PTO-413) Paper No(s)/Mail Date. _____.
5) ☐ Notice of Informal Patent Application (PTO-152)
6) ☐ Other: _____.

DETAILED ACTION

Claim Rejections - 35 USC § 103

1. The following is a quotation of 35 U.S.C. 103(a) which forms the basis for all obviousness rejections set forth in this Office action:

> (a) A patent may not be obtained though the invention is not identically disclosed or described as set forth in section 102 of this title, if the differences between the subject matter sought to be patented and the prior art are such that the subject matter as a whole would have been obvious at the time the invention was made to a person having ordinary skill in the art to which said subject matter pertains. Patentability shall not be negatived by the manner in which the invention was made.

2. Claims 1-2, 4, and 7-15 are rejected under 35 U.S.C. 103(a) as being unpatentable over Lee et al (US. 6,013,946) in view of Lupinski et al (US. 5,300,812).

Regarding claims 1-2, 4 and 5, Lee (Fig. 3) discloses a semiconductor device comprising: an integrated circuit semiconductor chip 130 having an active and a passive surface, the active surface including a protective adhesive layer 142, and at least one bonding pad 131; an electrically insulating substrate 120a having first and second surfaces; a plurality of electrically conductive routing strips 121 (not shown in Fig. 3, see Fig. 5) integral with the substrate; a plurality of contact pads 122 disposed on the first surface of the substrate, at least one of the contact pads electrically connected with at least one of the routing strips 121 (also see Fig. 5); the second surface of the substrate 120a being directly attached to the protective adhesive layer 142; and bonding wires 150 electrically connecting the at least one bonding pad 131 to at least one of the contact pads 122.

Lee does not disclose that the protective adhesive layer 142 is a protective polymer having been preactivated.

However, Lupinski teaches the forming of a protective polyimide polymer layer 40 being preactivated to impart adhesiveness between the semiconductor chip 30 and the insulating substrate 50 (see figure and column 7, lines 1-35). Accordingly, it would have been obvious to form the protective adhesive layer 142 of Lee with a polymer being preactivated, because as taught by Lupinski, such protective adhesive layer would provide void free adhesive bonding (column 2, lines 9-16).

Regarding claims 9-13, Lee's Fig. 3 further discloses: the bonding pad 131 disposed at the centerline of the chip 130; the substrate having an opening 123 and the contact pads disposed along the opening; the encapsulating material 161 covering the bonding wires 150 and the bonding pads 131 and the contact pads; and at least one solder ball 170 located on the assembly pads 122 and connected with one of the routing strips 121 (see Fig. 10).

Regarding claims 7-8, Lee further discloses the conventional device having bonding pad 52 disposed at the periphery of the chip 51 and the contact pads 54 disposed around the periphery of the substrate 53 (see Fig. 1).

Regarding claim 14, Lee does not disclose that the chip 130 and the substrate 120a have substantially the same outlines. However, it would have been obvious to form the chip 130 and the substrate 120a having the same outlines because changing in size/proportion of parts of an invention involves routine skill in the art. It has been held that where the only difference between the prior art and the claims was a recitation of relative dimensions of the claimed device and a device having the claimed relative dimensions would not perform differently than the prior art device, the claimed device

was not patentably distinct from the prior art device. *In Gardner v. TEC Systems, Inc.*, 725 F. 2d 1338, 220 USPQ 777 (fed. Cir. 1984), *Cert. Denied*, 469 U.S. 830, 225 USPQ 232 (1984).

3. Claims 5-6 are rejected under 35 U.S.C. 103(a) as being unpatentable over Lee et al and Lupinski et al as applied to claim 1 above, and further in view of Hiroshi (JP. 06-029454).

Neither Lee nor Lupinski disclose a metal layer disposed between the second surface of the substrate and the chip.

However, Hiroshi (Fig. 3) teaches the forming of a metal layer 2 on a protective adhesive layer 4, and between the second surface of the substrate 5 and the chip 1. Accordingly, it would have been obvious to modify the above combination device by forming a metal layer with the structure as set forth above, because as taught by Hiroshi, such modification would reduce the distorted stress from a lead layer (see translation, par. [0013]).

Allowable Subject Matter

4. Amended independent claim 3 is allowed.

(see reasons of the record).

Response to Arguments

5. Applicant argues that it would not be obvious to combine Lee with Lupinski because Lupinski does not suggest "a plurality of contact pads disposed on the first surface of the substrate and the second surface of the substrate being directly attached to the preactivated polymer level" (page 5 of Applicant's remark).

It should be noted that the rejection of the invention as claimed is not based on anticipation, but rather, is based on obviousness. Therefore, Applicant's argument above has no immediate apparent relevance to the issues presented by the rejection since Applicant cannot show nonobviousness by attacking references individually where the rejection is based upon a combination of references. *In re Young*, 403 F.2d 754, 757, 159 USPQ 725, 728 (CCPA 1968). The examiner relies on the combined teachings at Lee and Lupinski. Lupinski is not relied on for teaching a plurality of contact pads disposed on the first surface of the substrate and the second surface of the substrate being directly attached to the adhesive layer. Lee discloses a plurality of contact pads 122 disposed on the first surface of the insulating substrate 120 and the second surface of the insulating substrate 120 being directly attached to the adhesive layer 142 (see Fig. 3). Lupinski is relied on for showing that it was known to attach the active surface of a semiconductor chip 30 to an insulating substrate 50 by a preactivated polymer layer 40 for providing void free adhesive bonding (column 2, lines 9-16). Therefore, it would have been obvious to combine the references as suggested because Lupinski clearly suggest the motivation to combine. The examiner thus regards Applicant's assertions as constituting evidence that Applicant has failed to consider as a whole the prior art teachings disclosed by the combining of the references.

Conclusion

6. **THIS ACTION IS MADE FINAL.** Applicant is reminded of the extension of time policy as set forth in 37 CFR 1.136(a).

A shortened statutory period for reply to this final action is set to expire THREE MONTHS from the mailing date of this action. In the event a first reply is filed within TWO MONTHS of the mailing date of this final action and the advisory action is not mailed until after the end of the THREE-MONTH shortened statutory period, then the shortened statutory period will expire on the date the advisory action is mailed, and any extension fee pursuant to 37 CFR 1.136(a) will be calculated from the mailing date of the advisory action. In no event, however, will the statutory period for reply expire later than SIX MONTHS from the mailing date of this final action.

7. Any inquiry concerning this communication or earlier communications from the examiner should be directed to Phat X. Cao whose telephone number is (571) 272-1703. The examiner can normally be reached on Monday - Thursday.

If attempts to reach the examiner by telephone are unsuccessful, the examiner's supervisor, Wael Fahmy can be reached on (571) 272-1705. The fax phone number for the organization where this application or proceeding is assigned is 703-872-9306.

Information regarding the status of an application may be obtained from the Patent Application Information Retrieval (PAIR) system. Status information for published applications may be obtained from either Private PAIR or Public PAIR. Status information for unpublished applications is available through Private PAIR only. For more information about the PAIR system, see http://pair-direct.uspto.gov. Should you have questions on access to the Private PAIR system, contact the Electronic Business Center (EBC) at 866-217-9197 (toll-free).

PC
August 4, 2004

PHAT X. CAO
PRIMARY EXAMINER